AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A switching system that employs inductive current steering, comprising:

at least two elements whose respective secondary windings ~~that provide respective~~ generate inductive currents in connection with applying a differential signal across the at least two elements;

a steering component that directs the inductive currents to a switching component; and

a differential component associated with the switching component that employs the inductive currents to generate a differential output.

2. (Original) The system of claim 1, the at least two elements are transformers.

3. (Original) The system of claim 1, respective primary windings of the at least two elements are powered by a differential clock bus.

4. (Cancelled)

5. (Original) The system of claim 1, the inductive currents are 180 degrees out-of-phase.

6. (Original) The system of claim 1, one of the inductive currents is utilized to turn "on" a first switch of the differential component and the other inductive current is utilized to turn "off" a second switch of the differential component.

7. (Original) The system of claim 1, a differential clock bus is utilized to toggle the state of a first switch and a second switch of the differential component.

8. (Original) The system of claim 1, the differential component comprises at least one differential transistor pair.

9. (Original) The system of claim 8, the differential transistor pair comprises at least two of an Indium Phosphide (InP), a carbon-doped InP, an Indium Gallium Arsenide (InGaAs), a GaAs, an Aluminum Gallium Arsenide (AlGaAs) heterojunction bipolar transistor (HBT), a Silicon-Germanium (SiGe) bipolar transistor (BJT) and Field Effect Transistor (FET).

10. (Original) The system of claim 1 is employed in one or more of a register, a flip-flop, a frequency divider, a memory module, a latch, a multiplexer, an oscillator, a power amplifier, an RF integrated circuit, and an ASIC.

11. (Original) The system of claim 1, the differential output is employed to drive a logic gate.

12. (Currently Amended) A switching system that utilizes inductive current steering, comprising:

a current steering component that generates activating and deactivating signals by inducing current in a secondary winding when a primary winding is energized by a signal from a single clock bus; and

a switching component that receives the activating and deactivating signals and generates a differential output based on the activating and deactivating signals.

13. (Original) The system of claim 12, the current steering component comprises a transformer.

14. (Cancelled)

15. (Currently Amended) The system of claim 12, a the secondary winding ~~associated with the current steering component~~ is center-tapped, the center tap is coupled to a current source, and a first and a second end of the secondary winding provide the activating and deactivating signals to the switching component.

16. (Original) The system of claim 12, the activating and deactivating signals are 180 degrees out-of-phase.

17. (Original) The system of claim 12, the activating signal facilitates generating a high output and the deactivating signal facilitates generating an opposite polarity low output of the differential output.

18. (Original) The system of claim 12, the switching component comprises a differential transistor pair.

19. (Original) The system of claim 12 is employed in one or more of a register, a flip-flop, a frequency divider, a memory module, a latch, a multiplexer, an oscillator, a power amplifier, an RF integrated circuit, and an ASIC.

20. (Currently Amended) A data track and hold system that employs inductive current switching, comprising:

at least two data latches; and

a transformer based clock bus that controls the at least two data latches *via* inductive current, the transformer based clock bus comprises at least one transformer for each respective transistor of the at least two data latches, respective transformers provide inductive current to respective transistors, and the inductive current defines the state of the respective transistors.

21. (Original) The system of claim 20, respective data latches comprise a track differential transistor pair and a hold differential transistor pair.

22. (Cancelled).

23. (Original) The system of claim 20 is employed as a D-flip-flop.

24. (Withdrawn) A shift register that employs inductive current switching, comprising: a plurality of flip-flops; and a clock bus that induces current, which defines state of respective flip-flops.

25. (Withdrawn) The system of claim 24, the plurality of flip-flops is serially coupled via routing at least one output of one flip-flop to at least one input of a succeeding flip-flop.

26. (Withdrawn) The system of claim 24, at least one flip-flop is configured with a fanout of one.

27. (Withdrawn) The system of claim 24, the clock bus comprises at least one transformer that generates the induced current.

28. (Currently Amended) A method for steering inductive current through one or more differential transistor pairs, comprising:

transmitting a clock signal over one of a single clock bus or a differential clock bus;

~~receiving a clock signal~~;

conveying the clock signal through [[on]] one or more transformers to generate one or more inductive currents; and

providing the one or more inductive currents to the one or more differential transistor pairs.

29. (Cancelled)

30. (Original) The method of claim 28, the one or more inductive currents comprise at least two currents that are 180 degrees out of phase with respect to one another.

31. (Original) The method of claim 28, the one or more inductive currents can be toggled *via* the clock signal in order to toggle the state of the one or more differential transistor pairs.

32. (Withdrawn) A inductive current-based data latching method, comprising: coupling at least two data latches in series; employing a transformer based clock bus that induces current; and routing the induced current to the at least two data latches to track and hold data within the data latches.

33. (Withdrawn) The method of claim 32 is employed in connection with one or more of a register, a flip-flop, a frequency divider, a memory module, a latch, a multiplexer, an oscillator, a power amplifier, an RF integrated circuit, and an ASIC.

34. (Currently Amended) A system that provides inductive current to a differential transistor pair, comprising:

means for receiving [[a]] <u>one of a single or a differential</u> clock signal;

means for generating an inductive current based on the clock signal; and

means for steering the inductive current through the differential transistor pair.